LOYOLA COLLEGE (AUTONOMOUS), CHENNAI – 600 034

B.C.A. DEGREE EXAMINATION – **COMPUTER APPLICATIONS**

SECONDSEMESTER – APRIL 2017

CA 2505- DIGITAL LOGIC FUNDAMENTALS

Date: 05-05-2017 Dept. No. Max. : 100 Marks
Time: 01:00-04:00

PART-A

Answer ALL of the following: **(10 X 2 = 20 Marks)**

1. Convert decimal 41 to binary.

2. Write the duality principle of Boolean algebra.

3. What are the different types of ROMs?

4. Implement the half adder with one exclusive-OR and an AND gate.

5. Draw the block diagram of PLA.

6. What is binary counter?

7. What are the 3 major phases of an instruction cycle?

8. Define Effective address.

9. What is interrupt cycle?

10. What is DMA?

PART-B

Answer ALL of the following: **(5 X 8 = 40 Marks)**

11 a) Write down the octal and hexadecimal equivalent of $(10110001101011.111100000110)_2$

(OR)

b) Express the Boolean function F = A+ B'C in a sum of minterms.

12 a) Derive the sum & carry Boolean expression for full adder.

(OR)

b) Explain a 3-to-8 line decoder with neat diagram.

13 a) Explain JK flip-flop in detail.

(OR)

b) Design a sequential circuit with 4 flip-flops A, B, C and D. The next states of B, C and D are equal to the present states of A, B and C respectively. The next state of A is equal to the exclusive-OR of the present states of C and D.

14 a) Design a PLA for fulladder.

(OR)

b) List the various registers and briefly describe their functions.

15 a) Explain vectored & non-vectored interrupt in detail.

(OR)

b) Draw block diagram of 8-bit ALU with 4 bit status register.

PART-C

Answer any TWO of the following: **(2 X 20 = 40 Marks)**

16 i) Simplify the boolean function $F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$

ii) Explain NAND as a universal gate.

17 i) Explain 4-bit binary ripple counter in detail.

ii) Explain timing & control in detail.

18 i) Design an accumulator with logic circuit .

ii) Explain instruction format with an example.

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