LOYOLA COLLEGE (AUTONOMOUS), CHENNAI – 600 034

B.Sc. DEGREE EXAMINATION – **PHYSICS**

THIRD SEMESTER – **NOVEMBER 2016**

PH 3504/PH 3502/PH 5501 – ELECTRONICS - I

Date: 04-11-2016 Dept. No. Max. : 100 Marks

Time: 09:00-12:00

PART – A

Answer All Questions. **(10 x 2 = 20 marks)**

1. State Norton's Theorem.
2. What is a constant current source?
3. What is a multistage amplifier? State the role of coupling devices in such amplifiers.
4. A phase shift oscillator uses 5 pF capacitors. Find the value of R to produce a frequency of 800 kHz.
5. Define open loop gain of an amplifier.
6. What is the difference between D-MOSFET and E-MOSFET. For a D-MOSFET find I_D at V_{GS} = -3V given I_{DSS}=10mA and $V_{GS(off)}$ = -8V.
7. Draw the block diagram of a four-bit parallel binary adder.
8. Construct a D flip-flop by suitably modifying a clocked RS flip flop. Give its truth table.
9. What is a binary register? State its applications.
10. Construct a MOD-3 counter using JK flip flops.

PART – B

Answer ANY FOUR Questions. **(4 x 7.5 = 30 marks)**

11. State and explain superposition theorem. (1.5+6)
12. Explain the functioning of a Hartley Oscillator with a neat circuit diagram. (7.5)
13. Describe the construction and working of an n-channel FET. Plot its output characteristics. (5.5+2)
14. Simplify into sum of products F (A, B, C, D) = Σ (2,3,12,13,14,15) using K-map and draw the logic circuit for the simplified expression. (6+1.5)
15. Write short notes on memory devices ROM and RAM. (7.5)

PART C

Answer ANY FOUR questions. **(4 x 12.5 = 50 marks)**

16. Obtain expressions for the input impedance, current gain, voltage gain and output impedance in terms of hybrid parameters using the equivalent circuit of a transistor in CE configuration. (12.5)
17. Describe with the relevant circuit diagram the biasing of a transistor using the voltage divider biasing technique. (12.5)
18. Construct a circuit consisting of opamps that will solve the simultaneous equations, $ax + by = p$; $cx – dy = q$. (12.5)

19. (a) Explain the working of a JK flip flop with the logic diagram and truth table.

(b) Draw the logic circuit of a 1 to 4 demultiplexer and explain its operation with the truth table. (6+6.5)

20. (a) Explain the working of a 4 bit binary down counter using JK flip flops.

(b) Explain the operation of shifting a four bit data into a four bit register. (6+6.5)

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